Notice of Allowability	Application No.	Applicant(s)	
	10/762,973	WEIS, ROLF	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment of 7/16/2004*.

2. ☒ The allowed claim(s) is/are *1-41*.

3. ☒ The drawings filed on *22 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL..

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 1/22/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This action is in response to applicant's amendment of 7/16/2004.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Barry W. Dove on July 16, 2004.

Please replace Claims 1, 34 and 40 with revised Claims 1, 34 and 40 as shown below:

1. A method for forming an alignment mark structure using standard process steps for forming a vertical gate transistor, comprising the steps of:

forming a deep trench stud in an alignment mark region concurrently with a formation of a vertical gate transistor electrode in a circuit region, wherein the deep trench stud is formed from the same material as the vertical gate transistor electrode;

etching the stud to reduce a top area of the stud and forming an isolation trench in the alignment mark region adjacent to the stud, both concurrently with a formation of an isolation trench adjacent to the vertical gate transistor electrode in the circuit region;

filling the alignment mark isolation trench with an insulating material while filling the circuit region isolation trenches with the insulating material; and

removing a portion of the insulating material from the alignment mark isolation trench to a level below the top of the stud so that an upper portion of the stud extends above the insulating material, concurrently with a removal of a portion of the insulating material from the circuit region isolation trenches.

34. A method for forming an alignment mark structure using standard process steps for forming a vertical gate transistor, comprising the step of:

forming a deep trench stud that extends above an adjacent surface in an alignment mark region, concurrently with a formation of a vertical gate transistor electrode in a circuit region, wherein the deep trench stud is formed from the same material as the vertical gate transistor electrode.

40. A method for aligning a mask with prior formed structures in an active area of a circuit region when an alignment mark region is covered by an opaque material layer, the method comprising the steps of:

forming an alignment mark structure in the alignment mark region using standard process steps for forming a vertical gate transistor, the forming alignment mark structure step comprising the steps of:

forming a deep trench stud in an alignment mark region concurrently with a formation of a vertical gate transistor electrode in a circuit region, wherein the deep trench stud is formed from the same material as the vertical gate transistor electrode, etching the stud to reduce a top area of the stud and forming an isolation trench in the alignment mark region adjacent to the stud, both concurrently with a formation of an isolation trench adjacent to the vertical gate transistor electrode in the circuit region,

filling the alignment mark isolation trench with an insulating material while filling the circuit region isolation trenches with the insulating material, and

removing a portion of the insulating material from the alignment mark isolation trench to a level below the top of the stud so that an upper portion of the stud extends above the insulating material, concurrently with a removal of a portion of the insulating material from the circuit region;

forming the opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region;

viewing the alignment mark structure through the mask, wherein a step feature formed by the stud is still present after the opaque material layer covers the alignment mark structure; and

aligning an alignment mark portion of the mask with the alignment mark structure.

Allowed Subject Matter

3. Claims 1 – 41 are allowed.

4. The following is an examiner's reason for allowance.

Zhang et al. (US 6,303,458) discloses (Figure 4B) a method where an alignment mark region having a stud formed of semiconductor material; an isolation trench partially filled with an oxide adjacent to the stud, wherein a step is formed having a height, being the distance from the top of the semiconductor stud to the top of the oxide in the adjacent isolation trench.

The prior art does not teach or fairly suggest, in combination with the other claimed features, a method for forming an alignment mark structure using standard process steps for forming a vertical gate transistor, comprising the step of: forming a deep trench stud that extends above an adjacent surface in an alignment mark region, concurrently with a formation of a vertical gate transistor electrode in a circuit region, wherein the deep trench stud is formed from the same material as the vertical gate transistor electrode.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance".

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

Jang et al. (US 6,049,137) teaches a method of forming a readable alignment mark structure using CMP.

Yen et al. (US 5,897,371) teaches an alignment mark structure and process of making compatible with chemical mechanical polishing.

Deconinck (US 6,030,897) teaches a method of forming an alignment mark structure.

Jang et al. (6,080,635) teaches a method of photo alignment for shallow trench isolation.

Diewald et al. (US 20030157779 A1) teaches a method for applying adjusting marks on a semiconductor disc.

Ackmann et al. (US 6,271,602 B1) teaches a method for reducing the damage an alignment mark formed in a semiconductor substrate due to chemical mechanical polishing.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WCV

Art Unit 2813

July 20, 2004

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER